

FIG. 3

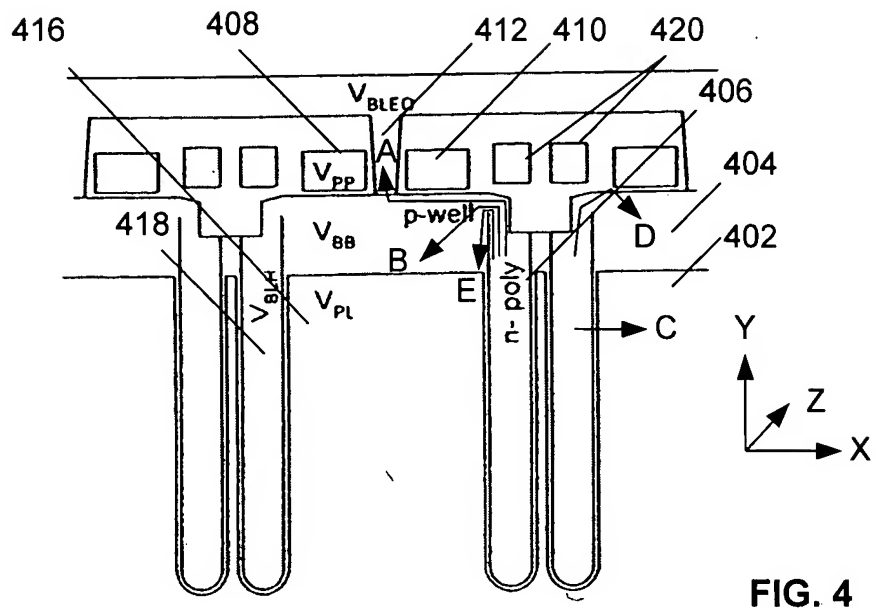


FIG. 4

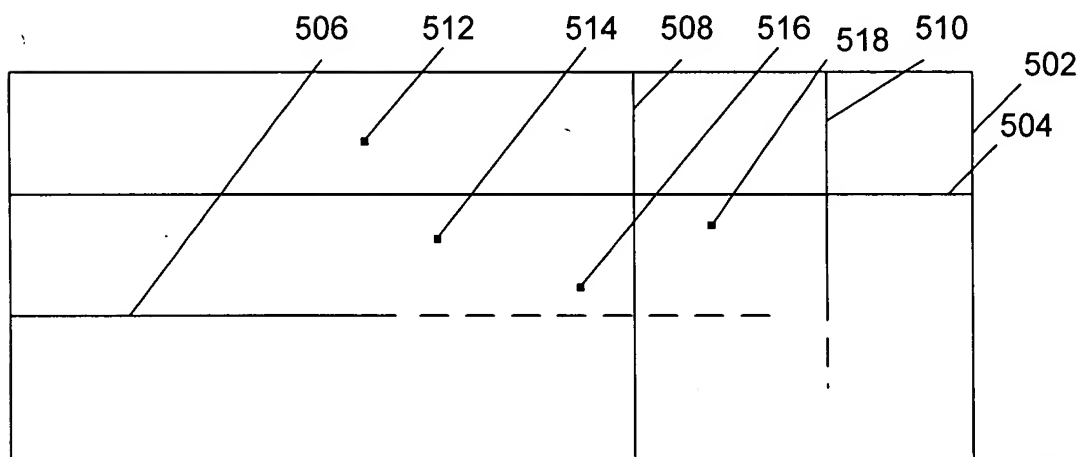


FIG. 5

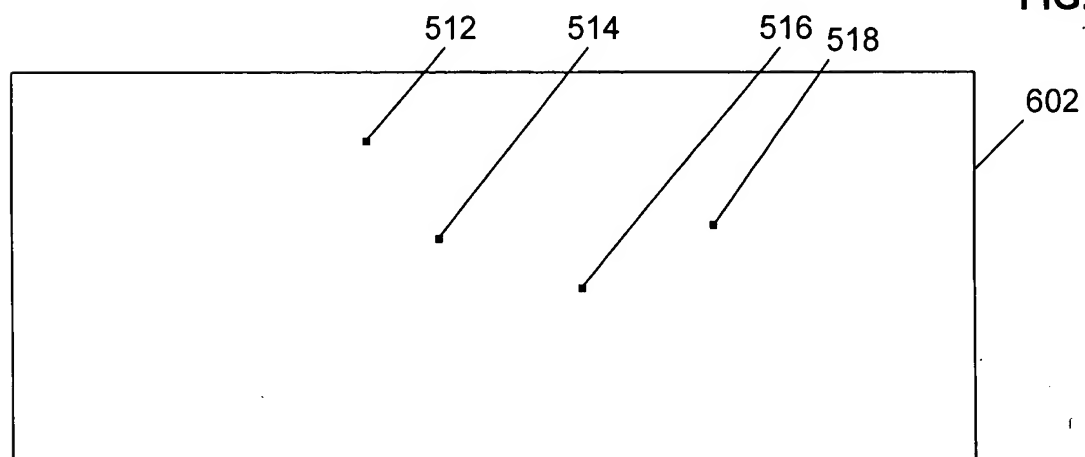


FIG. 6

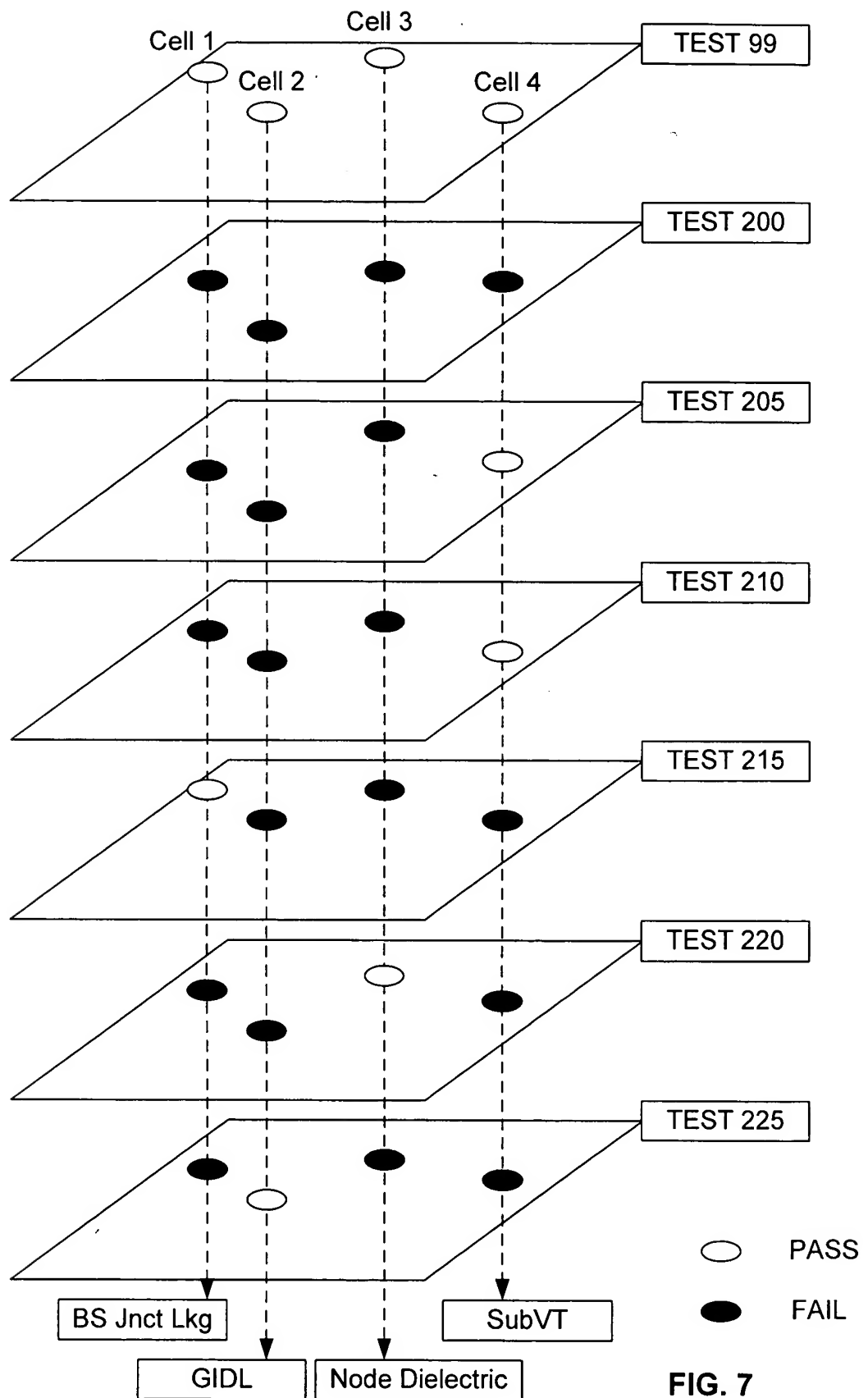


FIG. 7

		Test Conditions						identified					
test	Testname	$t_{RET}$ [ms]	bumped?	PWELL $V_{bb}$ [V]	Plate $V_{pl}$ [V]	Bitline Equalize $V_{bleq}$ [V]	Bitline High $V_{blh}$ [V]	BSJ/GIDL	BS Jctn. Lkg.	GIDL	Node Dief.	subVt	vert. FET
99	3VFCN	<<tRET	no	Vbb	Vpl	Vbleq	Vblh	0	0	0	0	0	0
200	SIGA0 (nominal)	tRET	no	Vbb	Vpl	Vbleq	Vblh	1	1	1	1	1	1
205	SIGA1	tRET	yes	Vbb-dVbb	Vpl	Vbleq	Vblh	1	1	1	1	0	0
210	SIGA2	tRET	yes	Vbb+dVbb	Vpl+dVpl	Vbleq+dVbleq	Vblh	1	1	1	1	0	1
215	SIGA3	tRET	yes	Vbb+dVbb	Vpl	Vbleq	Vblh	0	0	1	1	1	1
220	SIGA4	tRET	no	Vbb	Vpl+dVpl	Vbleq	Vblh	1	1	1	0	1	0
225	SIGA5	tRET	yes	Vbb-dVbb	Vpl-dVpl	Vbleq	Vblh	0	1	0	1	1	0
230	SIGA6	tRET	no	Vbb	Vpl-dVpl	Vbleq	Vblh	X	X	X	X	X	X
330	SIGA7 (cum.)	n.a.	yes	n.a.	n.a.	n.a.	n.a.	X	X	X	X	X	X

FIG. 8

		Test Conditions						induced				
test	Testname	t <sub>RET</sub> [ms]	bumped?	PWELL V <sub>bb</sub> [V]	Plate V <sub>pl</sub> [V]	Bitline Equalize V <sub>bleq</sub> [V]	Bitline High V <sub>blh</sub> [V]	BS Jctn. Lkg.	GIDL	Node Diel.	subVt	vert. FET
99	3VFCN	<<tRET	no	Vbb	Vpl	Vbleq	Vblh	0	0	0	0	0
200	SIGA0 (nominal)	tRET	no	Vbb	Vpl	Vbleq	Vblh	0	0	0	0	0
205	SIGA1	tRET	yes	Vbb- dVbb	Vpl	Vbleq	Vblh	1	0	0	0	0
210	SIGA2	tRET	yes	Vbb+ dVbb	Vpl+ dVpl	Vbleq+ dVbleq	Vblh	0	1	0	0	0
215	SIGA3	tRET	yes	Vbb+ dVbb	Vpl	Vbleq	Vblh	0	0	0	1	1
220	SIGA4	tRET	no	Vbb	Vpl+ dVpl	Vbleq	Vblh	0	0	0	0	0
225	SIGA5	tRET	yes	Vbb- dVbb	Vpl- dVpl	Vbleq	Vblh	0	0	0	0	0
230	SIGA6	tRET	no	Vbb	Vpl- dVpl	Vbleq	Vblh	0	0	1	0	1
330	SIGA7 (cum.)	n.a.	yes	n.a.	n.a.	n.a.	n.a.	1	1	1	1	1

FIG. 9

